chip technology and IC modules, but can be easily applied to other technologies using these metal pad materials and special interlocking ("islands") grid structures.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of fabricating an integrated circuit and other devices on a substrate, the method comprising:

providing a general substrate or substrate module;

providing a substrate having a layer of dielectric, interlevel dielectric (ILD), or an interconnect line layer, or device contact region to P-N junctions

providing a first level of metal wiring being defined and embedded in a first layer of insulator;

depositing a blanket of passivating dielectric layer (IMD) over the defined said first level metal wiring layer;

patterning and etching the said passivating dielectric (IMD) to form special interlocking grid structures with open contact regions to underlying first level metal wiring;

depositing a blanket of a metal barrier layer;

patterning and defining the said metal barrier layer on top of the interlocking grid structures;

depositing a blanket of a metal layer for metal pad formation on top of the interlocking grid structures;

patterning and defining the said metal pad layer to form metal pads on interlocking grid structures;

repeating the above process steps to construct multilevel pad structures by this robust method to form metal pad contact structures for chips, IC's and other applications.

2. The method of claim 1, wherein said substrate is semiconductor single crystal silicon or IC module or any substrate that supports and utilizes said special interlocking grid structure, material stack for metal pad formation.

3. The method of claim 1, wherein said layers of passivating dielectric insulating material are composed of insulating, refractory materials, i.e., silicon oxide, silicon nitride, silicon oxynitride and polyimides.

4. The method of claim 1, wherein said layer of first level metal wiring is composed of conducting metal copper.

5. The method of claim 1, wherein the said special interlocking grid structure composed of passivating material provide improved adhesion properties to the pad metal stack consisting of the underlying metal, metal barrier layer and top metal pad layer.

6. The method of claim 1, wherein the metal barrier layer is on top of the said interlocking grid structure and can be the following material, i.e.,

tantalum nitride, with thickness from about 150 Angstroms.

7. The method of claim 1, wherein said metal layer for metal pad formation on top of the special said material stack is aluminum.

8. The method of claim 1, wherein the metal pad special interlocking grid structure and method is comprising of forming a copper underlayer, forming the key interlocking grid structures, forming the tantalum nitride barrier layer, and finally forming the aluminum pad structure.

9. The method of claim 1, wherein the special metal pad interlocking grid structure stack is made by a robust process and has a robust interlocking structure, increasing surface roughness and area for improved adhesion properties and can be fabricated out of conducting materials for improved conductivity.

10. The method of claim 1, wherein the conducting material layers form an interlocking metal pad structure for contacts in a wide variety of applications, e.g., chip technology, IC module technology, and various solid

state devices where an integrated electrical contact is necessary.

11. The method of claim 1, wherein multilevel metal special interlocking pad structures are fabricating by repeating the special integrated process described herein.

12. A method of fabricating an integrated circuit on a substrate, using a new and improved method for fabricating aluminum metal pad structures wherein a special interlocking grid structure, for improved adhesion, is produced by this process, the method comprising the following steps:

providing a silicon substrate or IC substrate module with integrated circuits therein;

providing a substrate having a layer of dielectric, interlevel dielectric (ILD), or an interconnect line layer, or device contact region to P-N junctions;

providing a first level of copper conducting wiring being defined and embedded in a first layer of insulator, silicon oxide;

depositing a blanket of passivating dielectric layer (IMD) over the defined said first level copper metal wiring layer;

patterning and etching the said passivating dielectric (IMD) to form special interlocking grid structures with open contact regions to underlying first level metal wiring;

depositing a blanket of a metal barrier layer, e.g., a thin layer of tantalum nitride;

patterning and defining the said metal barrier layer on top of the interlocking grid structures;

depositing a blanket of an aluminum metal layer for metal pad formation on top of the interlocking grid structures;

patterning and defining the said aluminum metal pad layer to form metal pads on interlocking grid structures;

repeating the above process steps to construct multilevel pad structures.by this robust method to form interlocking metal pad contact structures for chips, IC's and other applications.

13. The method of claim 12, wherein said substrate is semiconductor single crystal silicon or IC module or any substrate that supports and utilizes said special interlocking grid structure, material stack for metal pad formation.

14. The method of claim 12, wherein said layers of passivating dielectric insulating material are composed of insulating, refractory materials, i.e., silicon oxide, silicon nitride, silicon oxynitride and polyimides.

15. The method of claim 12, wherein said layer of first level metal wiring is composed of conducting metal copper.

16. The method of claim 12, wherein the said special interlocking grid structure composed of passivating material provide improved adhesion properties to the pad metal stack consisting of the underlying metal, metal barrier layer and top metal pad layer.

17. The method of claim 12, wherein the metal barrier layer is on top of the said interlocking grid structure and can be the following material, i.e., tantalum nitride, with thickness from about 150 Angstroms.

18. The method of claim 12, wherein said metal layer for metal pad formation on top of the special said material stack is aluminum.

19. The method of claim 12, wherein the metal pad special interlocking grid structure and method is comprising of forming a copper underlayer, forming the key interlocking grid structures, forming the tantalum nitride barrier layer, and finally forming the aluminum pad structure.

20. The method of claim 12, wherein the special metal pad interlocking grid structure stack is made by a robust process and has a robust interlocking structure , for good adhesion and conductivity, as proven by stress tests and has confirmed adhesion properties by gold wire bond pull tests, improving device, circuit reliability.

21. The method of claim 12, wherein the special metal pad interlocking grid structure stack is made by a robust process and has a robust interlocking structure, increasing surface roughness and area for improved adhesion properties and can be fabricated out of conducting materials for improved conductivity.

22. The method of claim 12, wherein multilevel metal spiel interlocking pad structures are fabricating by repeating the special integrated process described herein.

23. A method of fabricating an integrated circuit on a substrate, using a unique method for fabricating aluminum metallurgy pad structure layer and lines, vias and interconnect wiring for MOSFET CMOS, memory and logic devices, and IC modules is produced by this process, the method comprising the following steps:

providing a silicon substrate or IC substrate module with integrated circuits therein;

providing a substrate having a layer of dielectric, interlevel dielectric (ILD), or an interconnect line layer, or device contact region to P-N junctions;

providing a first level of copper conducting wiring being defined and embedded in a first layer of insulator, silicon oxide;

depositing a blanket of passivating dielectric layer (IMD) over the defined said first level copper metal wiring layer;

patterning and etching the said passivating dielectric (IMD) to form special interlocking grid structures with open contact regions to underlying first level metal wiring;

depositing a blanket of a metal barrier layer, e.g., a thin layer of tantalum nitride;

patterning and defining the said metal barrier layer on top of the interlocking grid structures;

depositing a blanket of an aluminum metal layer for metal pad formation on top of the interlocking grid structures;

patterning and defining the said aluminum metal pad layer to form metal pads on interlocking grid structures;

repeating the above process steps to construct multilevel pad structures by this robust method to form reliable metal pad contact, lines and interconnect wiring structures for chips, IC's, IC modules and other electrical contact applications, therein using this unique interlocking material stack for robust electrical contact or contacts, lines or interconnect wiring.

24. The method of claim 23, wherein said substrate is semiconductor single crystal silicon or IC module or any substrate that supports and utilizes said special interlocking grid structure, material stack for metal pad formation.

25. The method of claim 23, wherein said layers of passivating dielectric insulating material are composed of insulating, refractory materials, i.e., silicon oxide, silicon nitride, silicon oxynitride and polyimides.

26. The method of claim 23, wherein said layer of first level metal wiring is composed of conducting metal copper.

27. The method of claim 23, wherein the said special interlocking grid structure composed of passivating material provide improved adhesion properties to the pad metal stack consisting of the underlying metal, metal barrier layer and top metal pad layer.

28. The method of claim 23, wherein the metal barrier layer is on top of the said interlocking grid structure and can be the following material, i.e., tantalum nitride, with thickness from about 150 Angstroms.

29. The method of claim 23, wherein said metal layer for metal pad formation on top of the special said material stack is aluminum.

30. The method of claim 23, wherein the metal pad special interlocking grid structure and method is comprising of forming a copper underlayer, forming the key interlocking grid structures, forming the tantalum

nitride barrier layer, and finally forming the aluminum pad structure.

31. The method of claim 23, wherein the special metal pad interlocking grid structure stack is made by a robust process and has a robust interlocking structure , for good adhesion and conductivity, as proven by stress tests and has confirmed adhesion properties by gold wire bond pull tests, improving device, circuit reliability.

32. The method of claim 23, wherein the special metal pad interlocking grid structure stack is made by a robust process and has a robust interlocking structure, increasing surface roughness and area for improved adhesion properties and can be fabricated out of conducting materials for improved conductivity.

33. The method of claim 23, wherein multilevel bond pad structures are fabricating by repeating the special integrated process described herein.

34. A bond pad structure, comprising:

a semiconductor substrate;

a plurality of conductive bond pads formed over said semiconductor substrate;

a passivating layer formed over said bond pads, having multiple openings to each said bond pads;

a barrier layer formed over said passivating layer and in said openings;

a conducting pad formed over each said bond pad and over said barrier layer, whereby an upper surface of said conductive pad provides improved adhesion for subsequently formed bonds.

35. The bond pad structure of Claim 34, wherein said conductive bond pads are formed of copper.

36. The bond pad structure of Claim 34, wherein said passivating layer is selected from the group consisting of silicon oxide, silicon nitride and polyimide.

37. The bond pad structure of Claim 34, wherein said bond pad forms an interlocking grid array in the bond pad via contact region, which is approximately 100 by 100 microns square and the size of the island structures are from about 10 to 25 microns in width, approximately 4 microns in height, and from about 4 to 10 in number, per said conducting bond pad, increasing surface area for improved adhesion.

38. The bond pad structure of Claim 34, wherein said conductive bond pads are formed of aluminum.

39. The bond pad structure of Claim 34, wherein said barrier layer is formed of tantalum nitride.